

VECTOR CONTROL UNIT

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REVISION HISTORY

REV	DATE	PAGES AFFECTED
B.01-B.02	8-15-84	ALL PAGES, ORIGINAL RELEASE
C.7	10-29-84	ALL PAGES - NEW LOCATIONS FOR REV. C. PLACEMENT
D.1	11-19-84	VCU.1,8,14,15 ISIS.1,2,3 LSCTL.1,2,3 LDSTCTL.1,2 MCTL.1,2,3 ACTL.1,2,3

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DEFINE
FIRST
XREF



CONVEX

TITLE: UCU

DRAWING: 410-000128-300 REV D.1

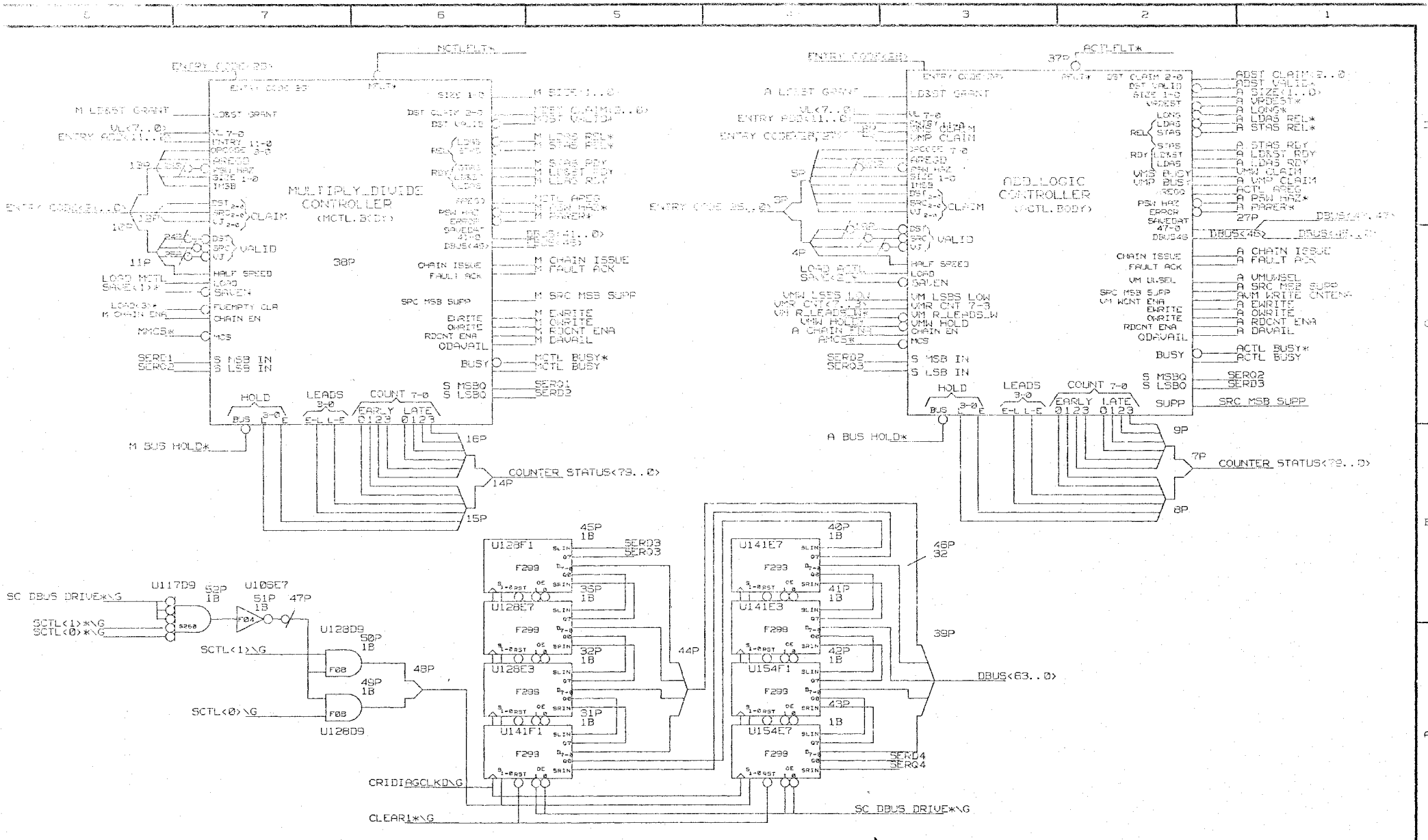
ABBR: UCU

ENGR: GRUGER

REVISED: Mon Nov 19 11:43:51 1984

PAGE:

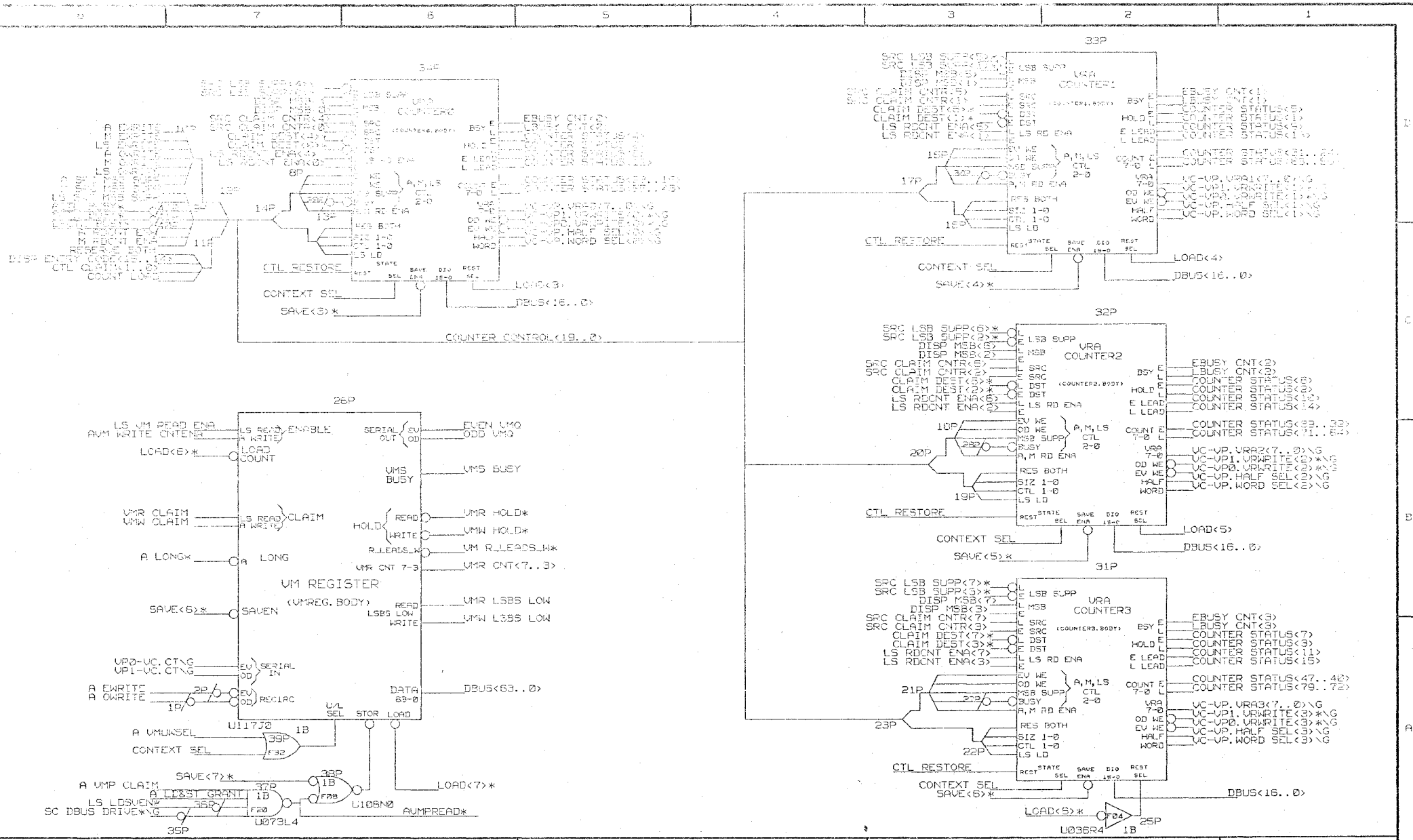
VCU.1 OF 15



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TITLE:	VCU	PBBR:	VCU
DRAWING:	410-000128-300 REV C.7	ENGR:	GRUGER
REVISED:	Tue Oct 9 10:07:13 1984	PAGE:	VCU.3

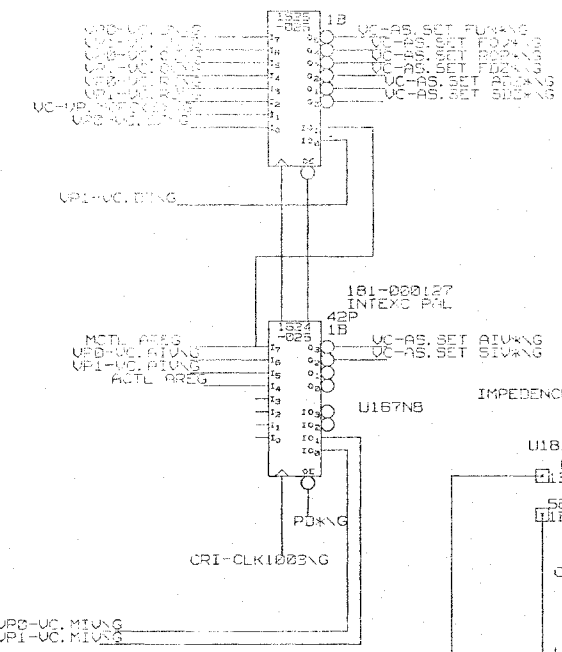
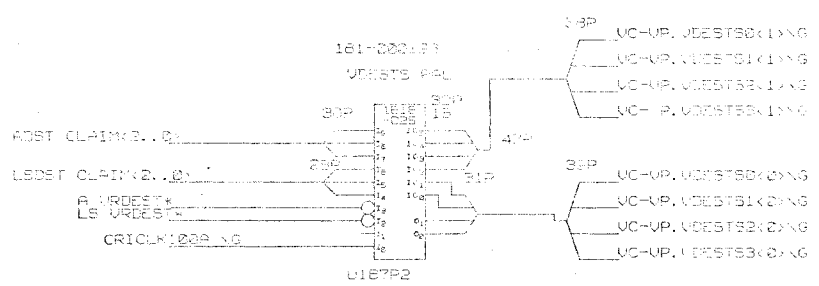


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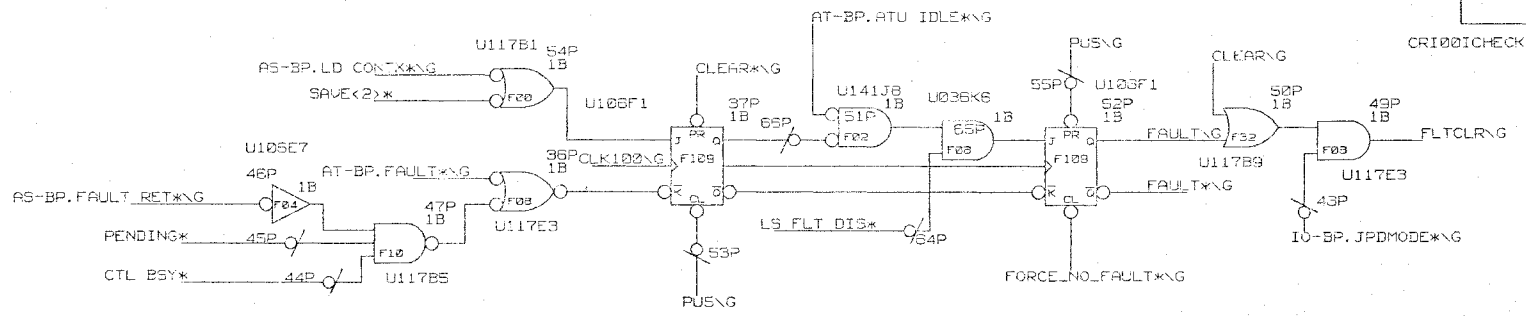
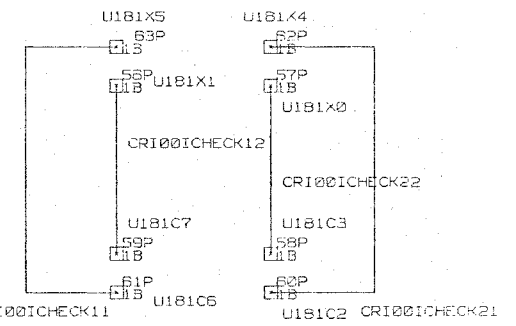
TITLE:	UCU	ABBR:	UCU
DRAWING:	410-000128-300 REV C.7	ENGR:	GRUGER
REVISED:	Tue Oct 9 14:14:43 1984	PAGE:	UCU.4

FPEXC PAL 181-000193
41P
U18786



181-000197
INTEXC PAL
42P
U18785

IMPEDANCE CHECK PARAPHERNALIA



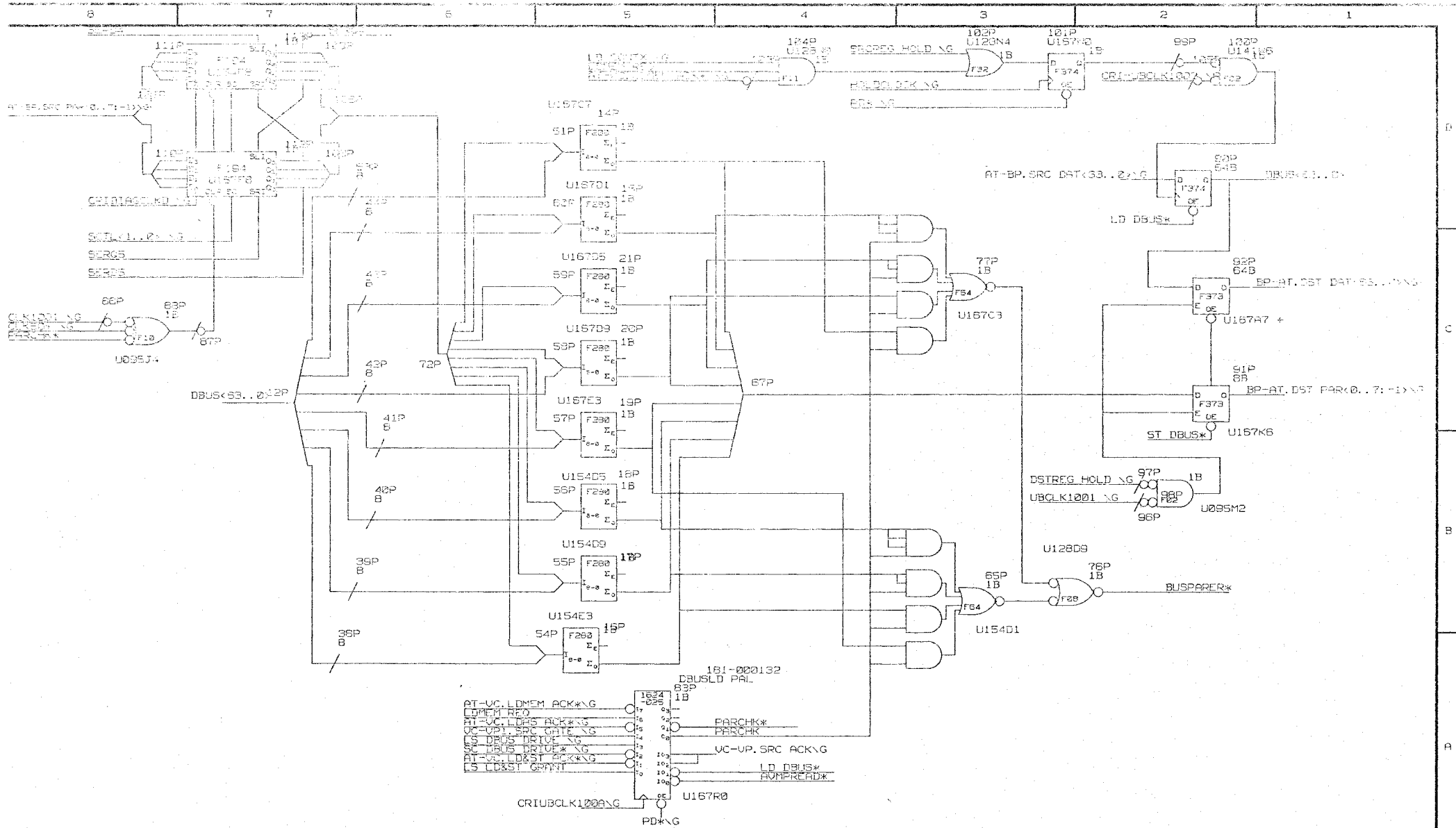
MISC. CONTROL LOGIC

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CONVEX

TITLE:	VCU	ABBR:	VCU
DRAWING:	410-000128-300 REV C.7	ENGR:	GRUGER
REVISED:	Fri Oct 12 14:12:35 1984	PAGE:	VCU.5
3	2	1	



PARITY LOGIC AND BUS INTERFACE

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CONVEX

TITLE:	VCU	ABBR:	VCU
DRAWING:	410-000128-300 REV C.7	ENGR:	GRUGER
REVISED:	Tue Oct 9 15:09:37 1984	PAGE:	VCU.7

IP
302-010990-310
U18509

A	B	C
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02	02	02
03	03	03
04	04	04
05	05	05
06	06	06
07	07	07
08	08	08
09	09	09
10	10	10
11	11	11
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24	24	24
25	25	25
26	26	26
27	27	27
28	28	28
29	29	29
30	30	30
31	31	31
32	32	32

CONNECTOR P1

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TITLE:	VCU	ABBR:	VCU
DRAWING:	410-000128-300 REV C.7	ENGR:	GRUGER
REVISED: Tue Oct 9 15:19:09 1984	PAGE:	VCU.9	

1P
302-010960-310
U18878

A	01	CONGND \NG
	02	AT-BP. SRC DAT<10>\NG
	03	AT-BP. SRC DAT<13>\NG
	04	AT-BP. SRC PAR<6>\NG
	05	BP-AT. DST DAT<10>\NG
	06	BP-AT. DST DAT<13>\NG
	07	BP-AT. DST DAT<15>\NG
	08	AT-BP. SRC DAT<41>\NG
	09	CONGND \NG
	10	AT-BP. SRC DAT<46>\NG
	11	BP-AT. DST DAT<40>\NG
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	13	BP-AT. DST DAT<46>\NG
	14	BP-AT. DST PAR<2>\NG
	15	UC-UP. URA2<5> \NG
	16	UC-UP. URA2<2> \NG
	17	CONGND \NG
	18	UC-UP. URA3<5> \NG
	19	UC-UP. URA3<2> \NG
	20	AT-BP. SRC DAT<16>\NG
	21	AT-BP. SRC DAT<19>\NG
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	25	CONGND \NG
	26	BP-AT. DST DAT<23>\NG
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	28	AT-BP. SRC DAT<52>\NG
	29	AT-BP. SRC DAT<55>\NG
	30	BP-AT. DST DAT<48>\NG
	31	BP-AT. DST DAT<51>\NG
	32	BP-AT. DST DAT<54>\NG

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	02	AT-BP. SRC DAT<11>\NG
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	15	UC-UP. URA2<4> \NG
	16	UC-UP. URA2<1> \NG
	17	UC-UP. URA3<7> \NG
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	19	UC-UP. URA3<1> \NG
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	21	AT-BP. SRC DAT<20>\NG
	22	AT-BP. SRC DAT<22>\NG
	23	BP-AT. DST DAT<16>\NG
	24	BP-AT. DST DAT<19>\NG
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	32	BP-AT. DST DAT<55>\NG

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	02	AT-BP. SRC DAT<12>\NG
	03	AT-BP. SRC DAT<15>\NG
	04	BP-AT. DST DAT<9>\NG
	05	CONGND \NG
	06	BP-AT. DST DAT<14>\NG
	07	AT-BP. SRC DAT<40>\NG
	08	AT-BP. SRC DAT<43>\NG
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	10	AT-BP. SRC PAR<2>\NG
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	13	CONGND \NG
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	15	UC-UP. URA2<3> \NG
	16	UC-UP. URA2<0> \NG
	17	UC-UP. URA3<6> \NG
	18	UC-UP. URA3<3> \NG
	19	UC-UP. URA3<0> \NG
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	21	CONGND \NG
	22	AT-BP. SRC DAT<25>\NG
	23	BP-AT. DST DAT<17>\NG
	24	BP-AT. DST DAT<20>\NG
	25	BP-AT. DST DAT<22>\NG
	26	AT-BP. SRC DAT<46>\NG
	27	AT-BP. SRC DAT<51>\NG
	28	AT-BP. SRC DAT<54>\NG
	29	CONGND \NG
	30	BP-AT. DST DAT<52>\NG
	31	BP-AT. DST DAT<53>\NG
	32	BP-AT. DST PAR<1>\NG

CONNECTOR R2

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CONVEX

TITLE:	ICU	REV:	1.0
DRAWING:	110-002188-500 REV. C.T	DATE:	07/87
REVISED:	110-002188-500	DATE:	07/87
REVISED:	110-002188-500	DATE:	07/87

1P

302-010960-310
U18SN7

A

01 CONGND \G

02 AT-BP.SRC DAT<2>\G

03 AT-BP.SRC DAT<5>\G

04 AT-BP.SRC PAR<7>\G

05 BP-AT.DST DAT<2>\G

06 BP-AT.DST DAT<4>\G

07 BP-AT.DST DAT<7>\G

08 AT-BP.SRC DAT<33>\G

09 CONGND \G

10 AT-BP.SRC DAT<38>\G

11 BP-AT.DST DAT<32>\G

12 BP-AT.DST DAT<35>\G

13 BP-AT.DST DAT<36>\G

14 BP-AT.DST PAR<3>\G

15 UC-UP.VDESTS1<1> \G

16 UC-UP.VDESTS2<0> \G

17 CONGND \G

18 UC-UP.HALF SEL<1> \G

19 UC-UP.WORD SEL<2> \G

20 UC-UP.ISRC<1> \G

21 UC-UP.USRCS1<0> \G

22 UC-UP.USRCS2<0> \G

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24 UC-UP.MSIS<1> \G

25 CONGND \G

26 UC-UP.MOPC<6> \G

27 UC-UP.MOPC<3> \G

28 UC-UP.MOPC<2> \G

29 UC-UP.AOPC<6> \G

30 UC-UP.AOPC<5> \G

31 UC-UP.AOPC<3> \G

32 UC-UP.AOPC<8> \G

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07 BP-AT.DST PAR<7>\G

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10 AT-BP.SRC DAT<39>\G

11 BP-AT.DST DAT<33>\G

12 BP-AT.DST DAT<36>\G

13 BP-AT.DST DAT<39>\G

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16 UC-UP.VDESTS3<1> \G

17 UC-UP.HALF SEL<3> \G

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19 UC-UP.WORD SEL<1> \G

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28 UC-UP.AOPC<10> \G

29 UC-UP.AOPC<7> \G

30 UC-UP.AOPC<5> \G

31 UC-UP.AOPC<2> \G

32 UC-UP.MIDOP \G

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01 AT-BP.SRC DAT<1>\G

02 AT-BP.SRC DAT<4>\G

03 AT-BP.SRC DAT<7>\G

04 BP-AT.DST DAT<1>\G

05 CONGND \G

06 BP-AT.DST DAT<6>\G

07 AT-BP.SRC DAT<32>\G

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12 BP-AT.DST DAT<37>\G

13 CONGND \G

14 UC-UP.VDESTS0<0> \G

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16 UC-UP.VDESTS3<0> \G

17 UC-UP.HALF SEL<2> \G

18 UC-UP.WORD SEL<3> \G

19 UC-UP.WORD SEL<0> \G

20 UC-UP.VSRC1<1> \G

21 CONGND \G

22 UC-UP.VSRC3<0> \G

23 UC-UP.MSIS<2> \G

24 UC-UP.ASIS<2> \G

25 UC-UP.ASIS<0> \G

26 UC-UP.MOPC<4> \G

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28 UC-UP.AOPC<9> \G

29 CONGND \G

30 UC-UP.AOPC<4> \G

31 UC-UP.AOPC<1> \G

32 UC-UP.AOPC \G

CONNECTOR P4

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CONVEX

TITLE:	UCL	REF:	UCL
BARCODE:	410-701096-800 REV 0.7	EXT:	07.007
REVISED:	Thu Oct 9 18:41:49 1984	PRICE:	UCL.11

8

7

6

5

4

3

2

1

IP
302-010960-310
U1B8T6

- A
- 01 CONGND NG
- 02 NC
- 03 NC
- 04 IP-BP. IREG<0>NG
- 05 IP-BP. IREG<1>NG
- 06 IP-BP. IREG<2>NG
- 07 NC
- 08 AT-BP. ATU IDLE*NG
- 09 CONGND NG
- 10 UC-AS. FAULT ACK* NG
- 11 UC-UP. MSRL<3> NG
- 12 UC-UP. MSRL<0> NG
- 13 UC-UP. ASRL<1> NG
- 14 UC-UP. MSROE<1> NG
- 15 UC-UP. ASROE<0> NG
- 16 UC-UP. MWAIT* NG
- 17 CONGND NG
- 18 IP-BP. OPND SIZ<1>NG
- 19 IP-UC. EP ADDR<2> NG
- 20 IP-UC. EP ADDR<5> NG
- 21 AS-VC. RUN SEQ* NG
- 22 UC-AS. SET ADZ* NG
- 23 UC-AS. SET FOU* NG
- 24 UC-AS. SET SIU* NG
- 25 CONGND NG
- 26 UC-AT. LD MEM REQ*NG
- 27 UC-AT. ST MEM REQ*NG
- 28 UC-UP. JSRC<1> NG
- 29 NC
- 30 AT-UC. LDAS ACK*NG
- 31 UC-UP1. MISC LAR*NG
- 32 UC-UP1. MT SRC SEL NG

- B
- 01 IP-VC. DISPATCH* NG
- 02 IP-VC. UP PSW HAZ*NG
- 03 NC
- 04 IP-BP. JREG<0>NG
- 05 IP-BP. JREG<1>NG
- 06 IP-BP. JREG<2>NG
- 07 NC
- 08 UC-IP. UCU RDY* NG
- 09 UC-AS. PSW HAZ* NG
- 10 AT-BP. FAULT*NG
- 11 UC-UP. MSRL<2> NG
- 12 UC-UP. ASRL<3> NG
- 13 UC-UP. ASRL<0> NG
- 14 UC-UP. MSROE<0> NG
- 15 UC-UP. OSWAPM NG
- 16 UC-UP. AWAIT* NG
- 17 IP-BP. OPND SIZ<0>NG
- 18 IP-VC. EP ADDR<0> NG
- 19 IP-VC. EP ADDR<3> NG
- 20 IP-VC. EP ADDR<6> NG
- 21 UC-UP. ASRC SWAP NG
- 22 UC-AS. SET FDE* NG
- 23 UC-AS. SET FUNK NG
- 24 UC-AS. SET AIV* NG
- 25 NC
- 26 UC-AT. LDAS REQ*NG
- 27 UC-UP. MERO SWAP NG
- 28 UC-UP. JSRC<0> NG
- 29 AT-UC. LD MEM ACK*NG
- 30 AT-UC. LDST ACK*NG
- 31 UC-UP1. ABCALARK*NG
- 32 UC-UP1. MT SRC SEL NG

- C
- 01 NC
- 02 NC
- 03 NC
- 04 IP-BP. KREG<0>NG
- 05 CONGND NG
- 06 IP-BP. KREG<1>NG
- 07 IP-BP. KREG<2>NG
- 08 AS-BP. ST CONTX*NG
- 09 AS-BP. LD CONTX*NG
- 10 AS-BP. FAULT RET*NG
- 11 UC-UP. MSRL<1> NG
- 12 UC-UP. ASRL<2> NG
- 13 CONGND NG
- 14 UC-UP. ASROE<1> NG
- 15 UC-UP. OSWAPP NG
- 16 UC-UP. OUTI REG EN NG
- 17 UC-UP. DST BUS HOLD* NG
- 18 IP-VC. EP ADDR<1> NG
- 19 IP-VC. EP ADDR<4> NG
- 20 IP-VC. EP ADDR<7> NG
- 21 CONGND NG
- 22 UC-AS. SET ROP* NG
- 23 UC-AS. SET SBZ* NG
- 24 UC-AS. UNUSED*NG
- 25 UC-AT. LDST REQ*NG
- 26 UC-AT. STAS REQ*NG
- 27 UC-AS. CTRU NG
- 28 UC-UP. OUTJ REG EN NG
- 29 CONGND NG
- 30 AT-UC. STAS ACK*NG
- 31 AT-UC. STAT ACK*NG
- 32 AT-UC. ST MEM ACK*NG

CONNECTOR P4

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CONVEX

TITLE: UCU
DRAWING: 410-000128-000 REV 017

REVISED: Tue Oct 9 10:58:27 1984

DATE:

FILE: UCU

REV: 017

UCU 12

8

7

6

3

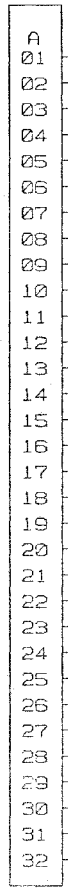
2

1

U002K5
10P
302-010950-310

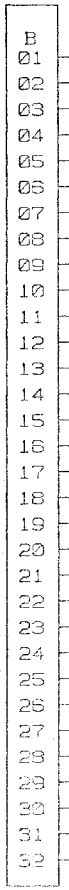
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ARE ADDED IN REV D.

VM SERIAL CLAIM
VM PARALLEL CLAIM
VL CLAIM
A REGISTER CLAIM



DISP ENTRY CODE<28, 27, 26, 17>

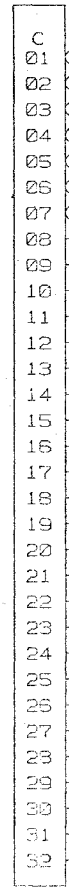
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ANXTAD<11..0> \G

MNXTAD<11..4> \G

LNXTAD<11..0> \G

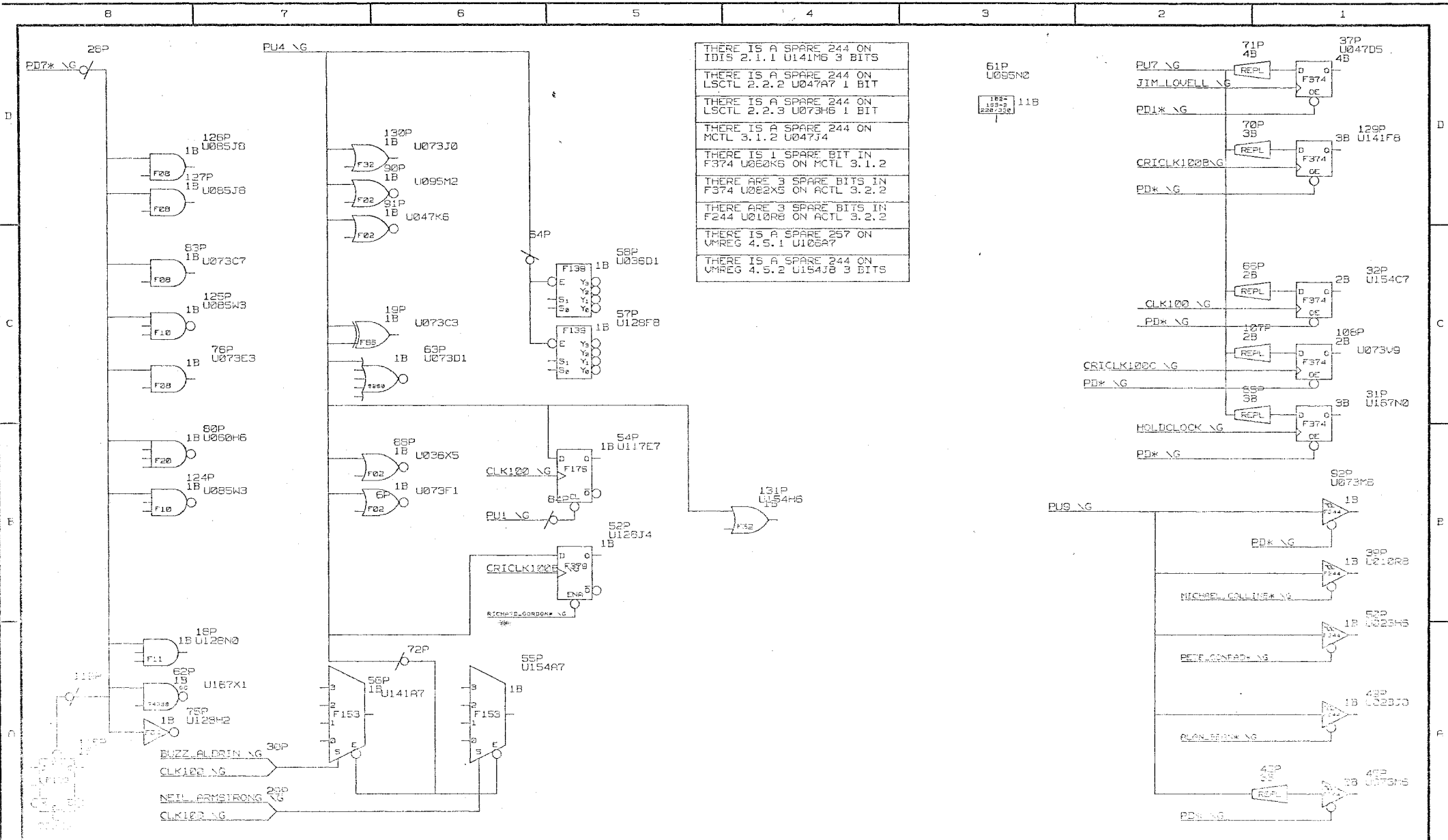


- 01 ACTL BUSY*
- 02 MCTL BUSY*
- 03 LSCTL BUSY*
- 04 PENDING*
- 05 M SCALAR BUSY*\G
- 06 A SCALAR BUSY*\G
- 07 LDST HAZ*
- 08 GND
- 09 VMS BUSY
- 10 25P
- 11 EBUSY CNT<3..0>
- 12
- 13
- 14 CTL CLAIM<1>
- 15 CTL CLAIM<0>
- 16 GND
- 17 24P
- 18 LBUSY CNT<3..0>
- 19
- 20
- 21 INST ISSUE
- 22 M CHAIN ISSUE
- 23 A CHAIN ISSUE
- 24 GND
- 25
- 26
- 27
- 28
- 29
- 30 22P
- 31 MNXTAD<1..0> \G
- 32 GND

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FORM: 010	REVISION: 000
DATE: 010-00105-000 REV. D.1	DATE: 01/19/84
BY: W. J. W. 01 10/19/84 1004	DATE: 01/19/84



THERE IS A SPARE 244 ON IDIS 2.1.1 U141M6 3 BITS
THERE IS A SPARE 244 ON LSCTL 2.2.2 U047A7 1 BIT
THERE IS A SPARE 244 ON LSCTL 2.2.3 U073H6 1 BIT
THERE IS A SPARE 244 ON MCTL 3.1.2 U047J4
THERE IS 1 SPARE BIT IN F374 U000K5 ON MCTL 3.1.2
THERE ARE 3 SPARE BITS IN F374 U002X5 ON ACTL 3.2.2
THERE ARE 3 SPARE BITS IN F244 U010R8 ON ACTL 3.2.2
THERE IS A SPARE 257 ON UMREG 4.5.1 U108A7
THERE IS A SPARE 244 ON UMREG 4.5.2 U154J8 3 BITS

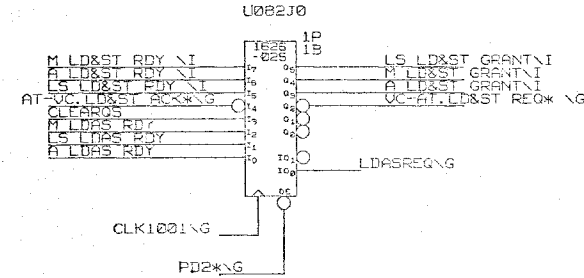
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TITLE: 400
 DRAWING: 400-00155-100 REV D.1
 REVISION: 1 1/2 10/87 BY: J. L. P. 1134 PAGE: 11/11

B 7 6 5 4 3 2 1

LDSTARB PAL
181-000134



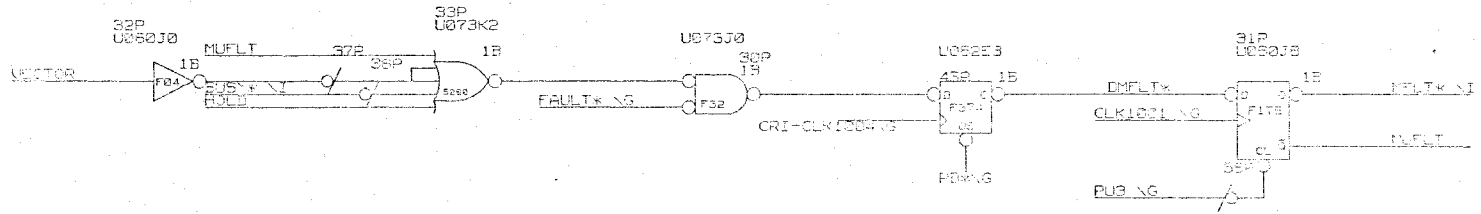
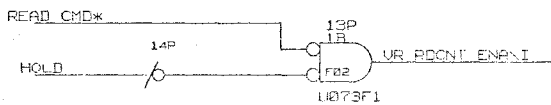
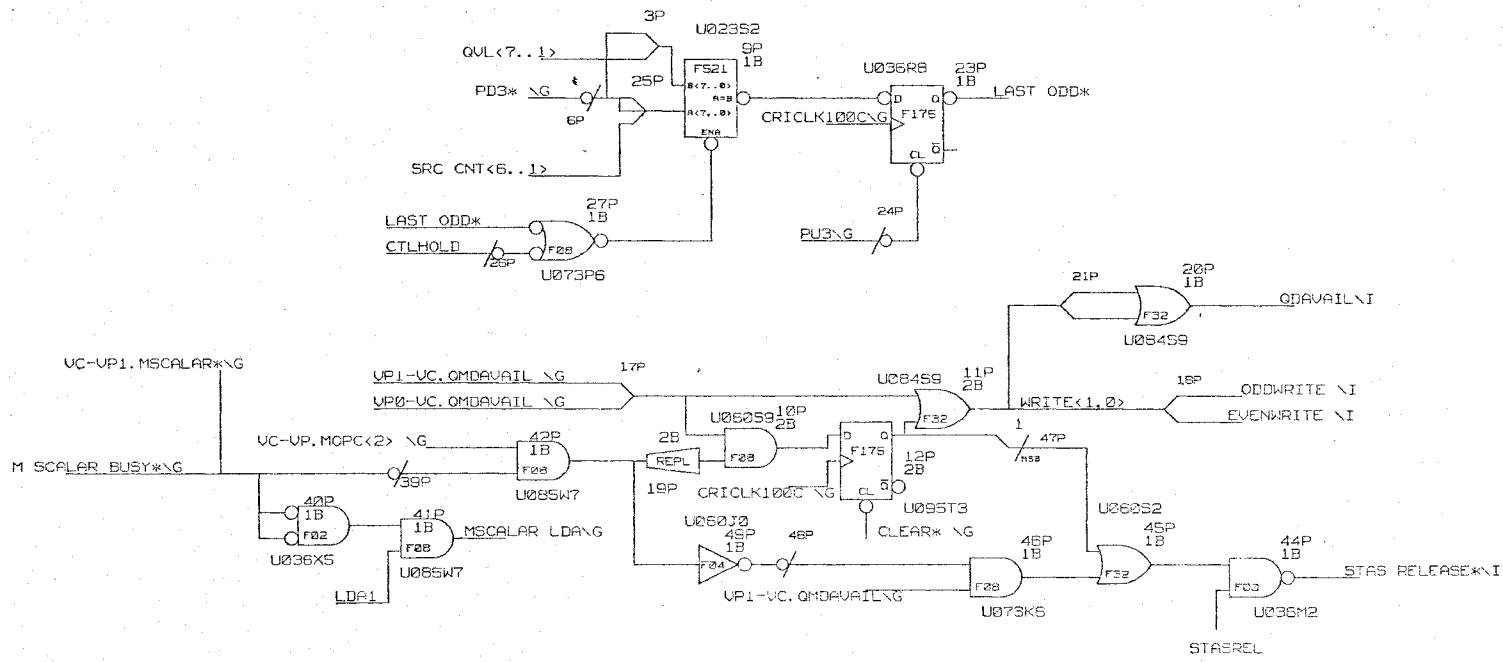
LOAD AND STORE BUS CONTROL

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TITLE: LDSTARB	ASST: LDSTARB
DRAWING: 410-000134-100 REV D.1	ENGR: GP/REP
DESIGNED: MCA 001 18 01 80: 7/ 1984	PRG: LDSTARB.2

E 7 6 5 4 3 2 1



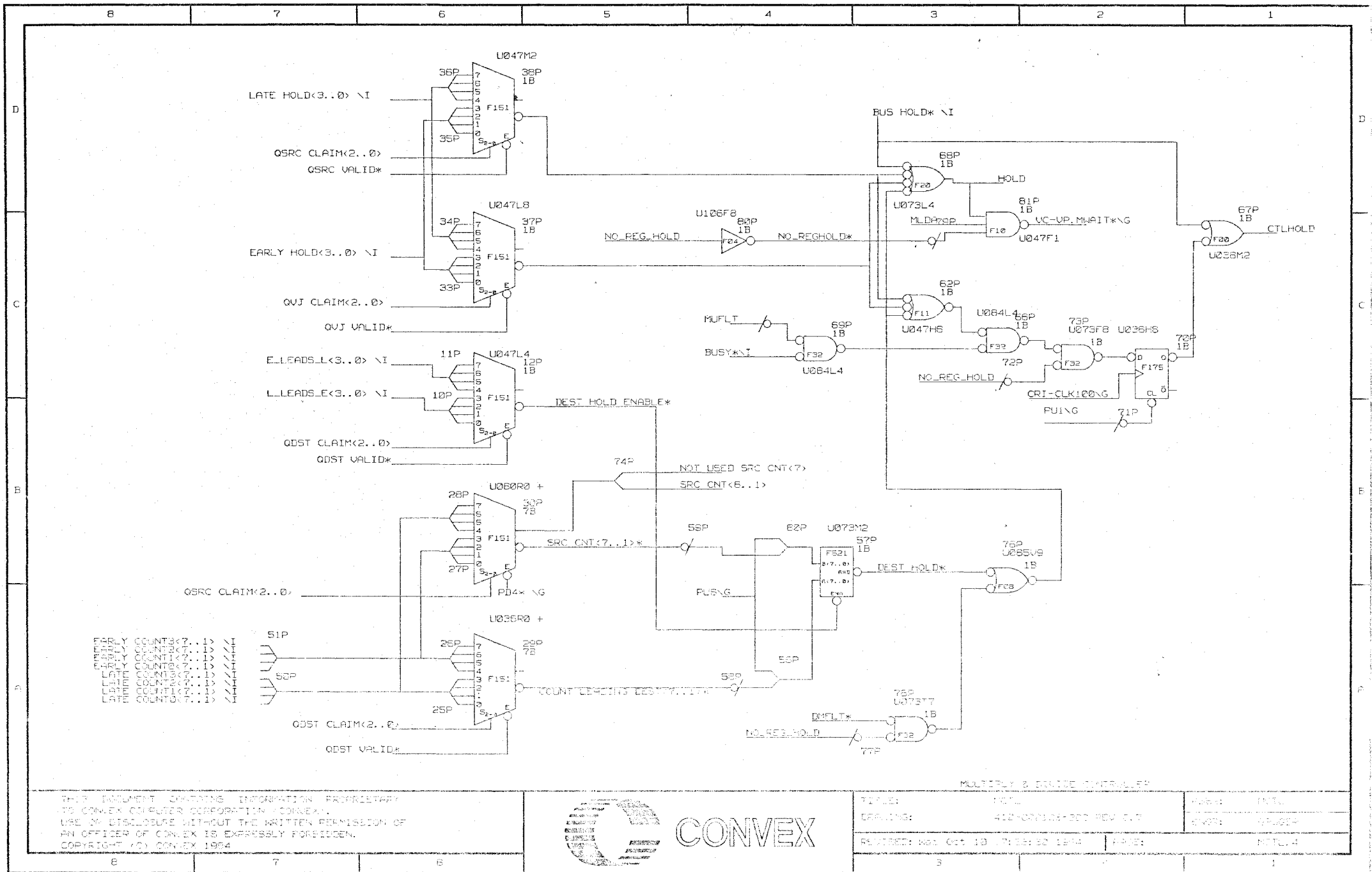
MULTIPLY & DIVIDE CONTROL

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DESIGN:	REV:	DATE:
DESIGNER:	REVISED BY:	DATE:
DESIGN NO. 18	REV. 001	1974
		PAGE 3



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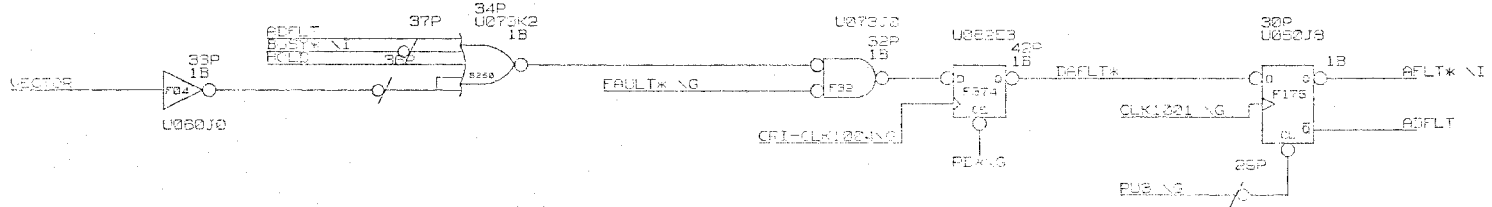
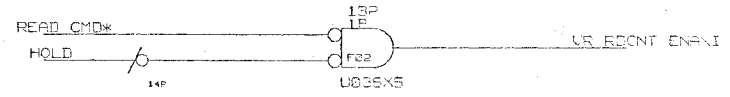
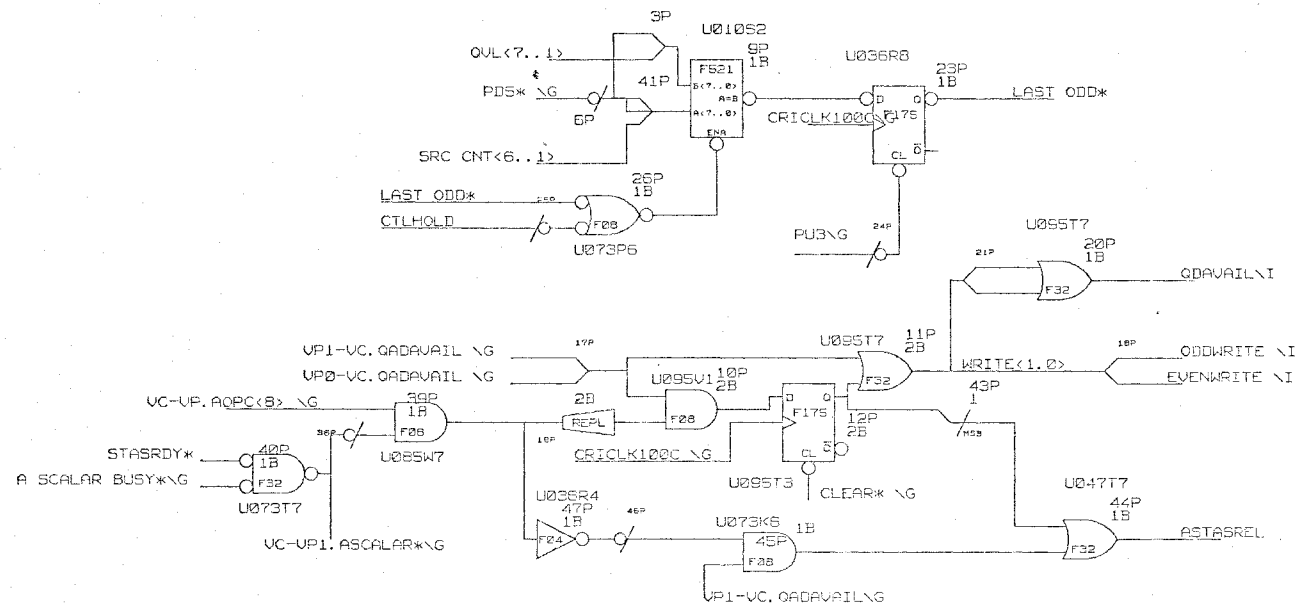
MULTIPLY & DIVIDE CONTROLLER	
TITLE:	101
DRAWING:	412-073100-300 REV 0.3
REVISED:	Wed Oct 10 11:55:30 1984
DATE:	10/10/84
FILE:	MTC1.4

D

C

B

A

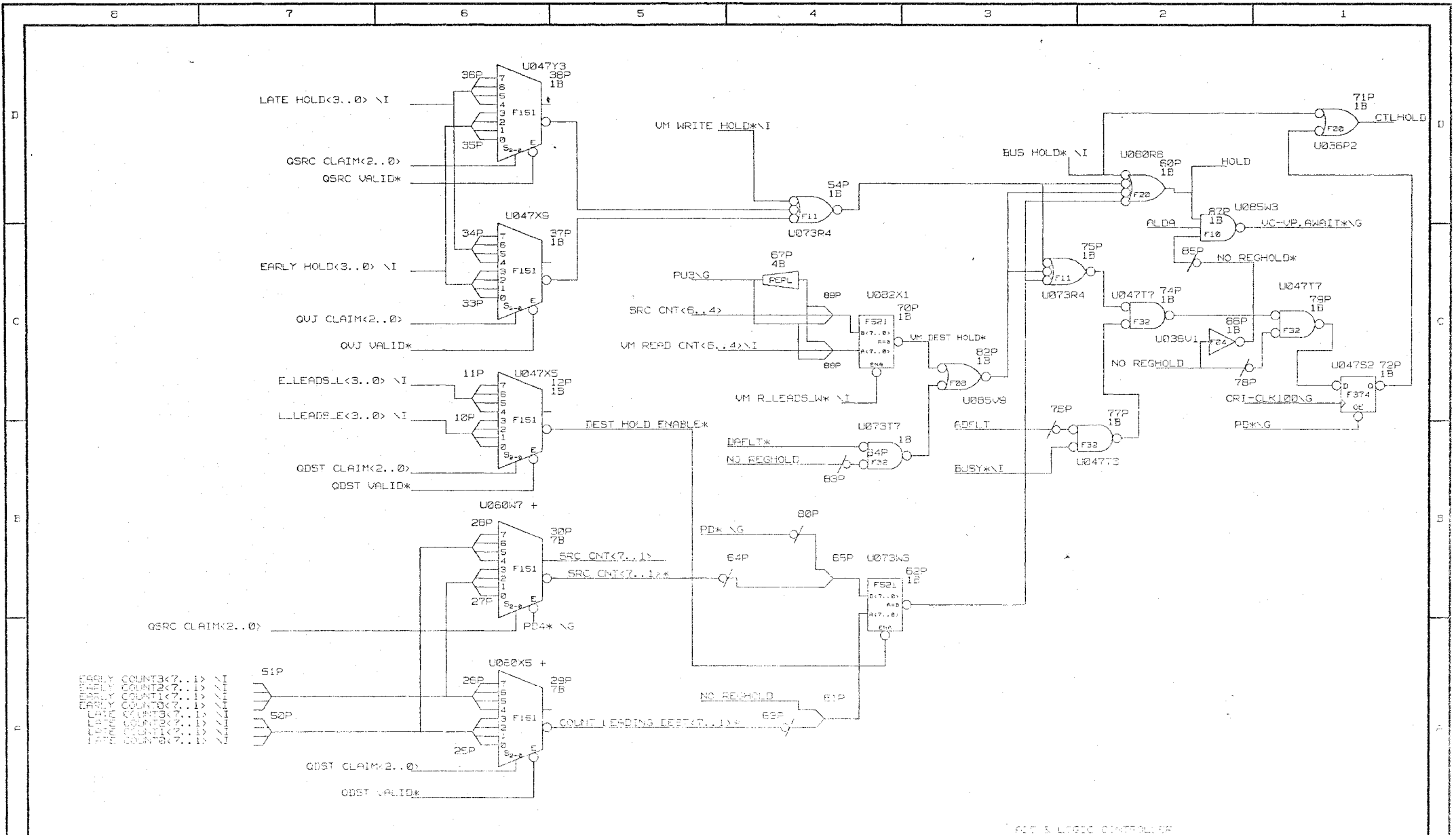


ASB & LOGIC CONTROL

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TITLE:	ASB	AREA:	FCPL
MARKING:	410-00118-000 REV D.1	ENGR:	GAJGCP
DATE:	MAY 19 1984	PAID:	FCPLB



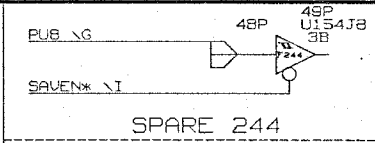
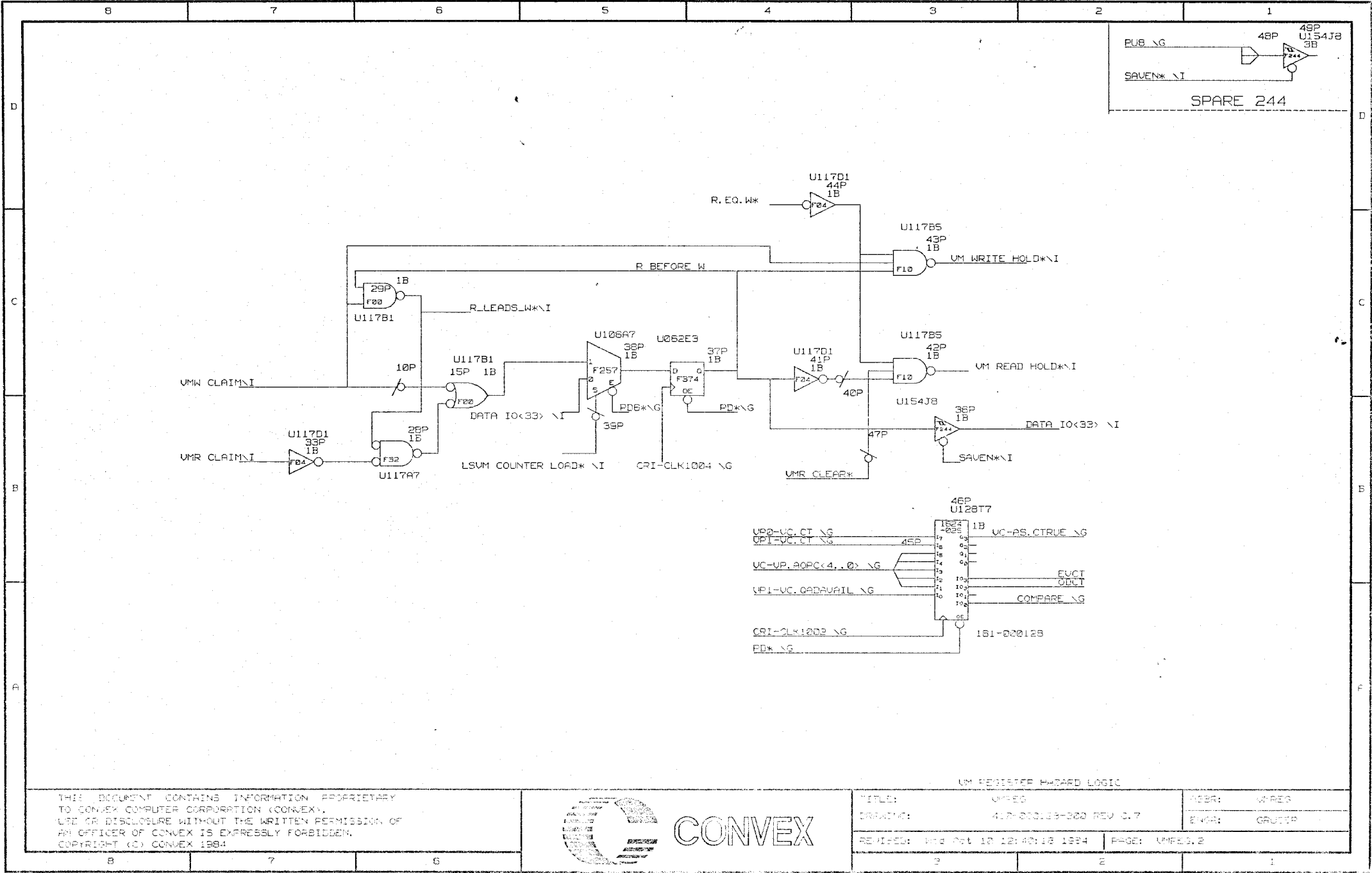
ALU & LOGIC CONTROLLER

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CONVEX

FILE:	ACPL	DATE:	ACPL
DRAWING:	ALU-LOGIC-100 REV. 1.7	BY:	GRUBER
REVISION:	ADD CRI TO 17:38:17 1984	DATE:	ACPL 84



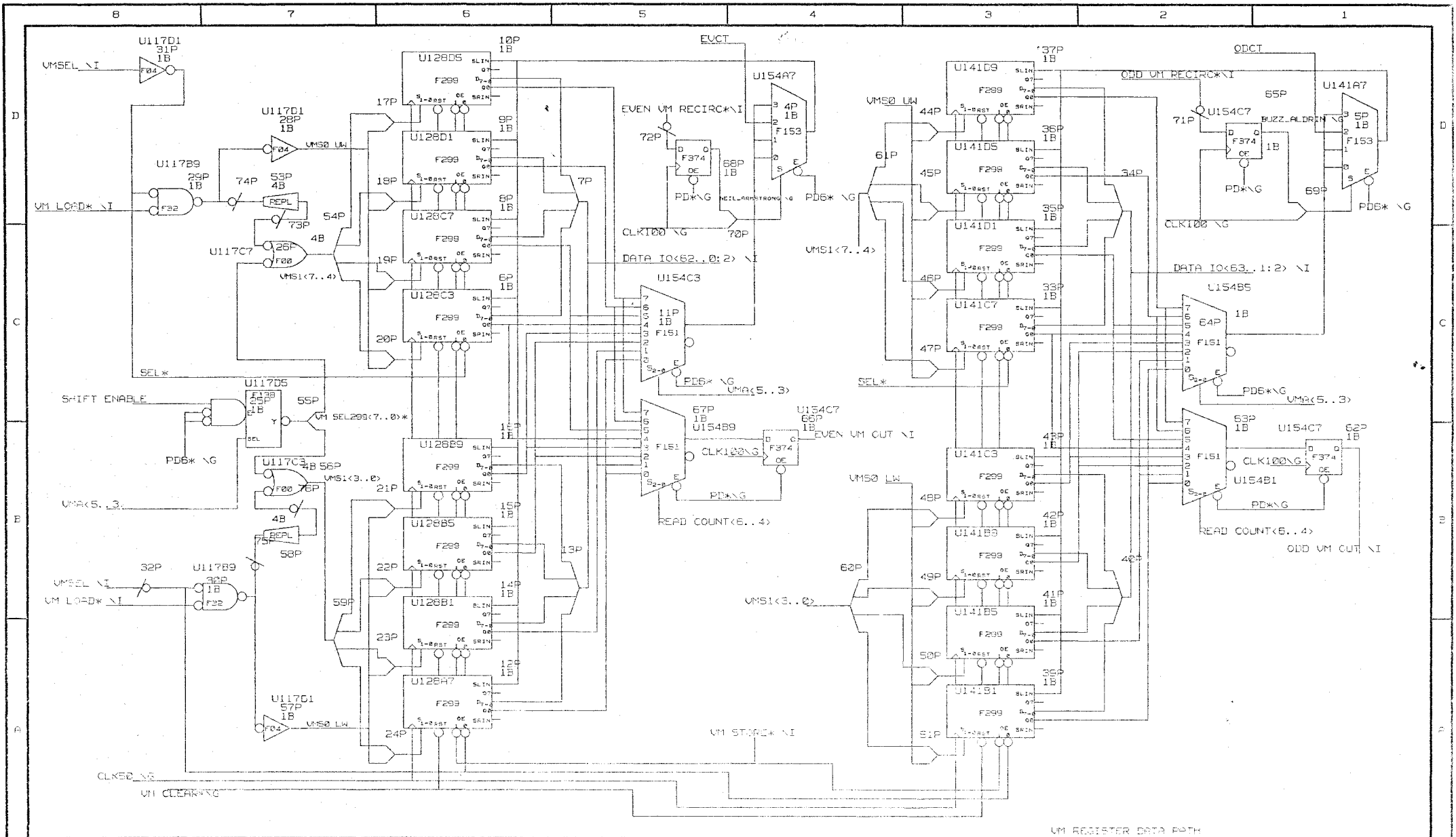
UMR REGISTER FORWARD LOGIC

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CONVEX

TITLE:	UMREG	REBR:	UPREG
DRAWING:	412-000125-000 REV 0.7	ENGR:	CRUTER
REVISED:	Wed Oct 10 12:40:18 1984	PAGE:	UMREG.2



UM REGISTER DATA PATH

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CONVEX

TITLE:	UM-03	REV:	0000
DRAWING:	410-000100-000 REV. 0.7	ENGR:	CAUSP
REVISED:	Wed Oct 17 17:50:38 1984	CODE:	UMREG.3